

IN THE CLAIMS

The following is a complete listing of the claims:

1. (original) A Schmitt trigger configured to receive an input voltage and produce an output voltage that changes states with respect to a high voltage threshold and a low voltage threshold, comprising:
  - a first feedback path configured to determine one of the voltage thresholds; and
  - at least one diode coupled to the first feedback path such that an on-current through the first feedback path is reduced as a supply voltage for the Schmitt trigger is reduced.
2. (original) The Schmitt trigger of claim 1, wherein the Schmitt trigger is a CMOS Schmitt trigger.
3. (original) The Schmitt trigger of claim 1, wherein the first feedback path is configured to determine the low voltage threshold, the Schmitt trigger further comprising: a second feedback path configured to determine the high voltage threshold.
4. (original) The Schmitt trigger of claim 3, wherein the first feedback path comprises a first PMOS transistor having a terminal coupled to the at least one diode and wherein the second feedback path comprises a first NMOS transistor.
5. (original) The Schmitt trigger of claim 4, wherein the at least one diode comprises a first diode and a second diode.

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6. (original) The Schmitt trigger of claim 4, wherein the terminal is a drain terminal, the at least one diode coupled between the drain terminal and a ground.
7. (original) The Schmitt trigger of claim 1, wherein the first feedback path determines the high voltage threshold, the Schmitt trigger further comprising: a second feedback path that determines the low voltage threshold.
8. (original) The Schmitt trigger of claim 7, wherein the first feedback path comprises a first NMOS transistor having a terminal coupled to the at least one diode and wherein the second feedback path comprises a first PMOS transistor.
9. (original) The Schmitt trigger of claim 8, wherein the at least one diode comprises a first diode and a second diode.
10. (original) The Schmitt trigger of claim 8, wherein the terminal is a drain terminal, the at least one diode coupled between the drain terminal and a supply voltage terminal.
11. (original) The Schmitt trigger of claim 4, further comprising a second and a third PMOS transistor and a second and a third NMOS transistor all coupled in series between a supply voltage terminal and a ground terminal.
12. (original) A method of altering the hysteresis for a Schmitt trigger, the hysteresis being defined with respect to a high voltage threshold and a low voltage threshold, the Schmitt trigger including a first feedback path that determines one of the voltage thresholds, the method comprising:

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changing a supply voltage for the Schmitt trigger; and

in response to the changed supply voltage, affecting an on-current through the first feedback path using at least one diode such that the determined voltage threshold satisfies a predetermined threshold.

13. (original) The method of claim 12, wherein the first feedback path determines the low voltage threshold, the adjusting the supply voltage act comprises lowering the supply voltage, and the affecting the on-current comprises reducing the on-current through the first feedback path such that the low voltage threshold is offset from ground by the predetermined threshold.

14. (original) The method of claim 12, wherein the first feedback path determines the high voltage threshold, the adjusting the supply voltage act comprises increasing the supply voltage, and the affecting the on-current comprises increasing the on-current through the first feedback path such that the high voltage threshold is offset from the supply voltage by the predetermined threshold.

15. (original) A Schmitt trigger configured to receive an input voltage and produce an output voltage that changes states with respect to a high voltage threshold and a low voltage threshold, comprising:

a first feedback path configured to determine one of the voltage thresholds; and

means for reducing an on-current through the first feedback path as a supply voltage for the Schmitt trigger is reduced.

16. (original) The Schmitt trigger of claim 15, wherein the first feedback path comprises a first PMOS transistor and the means for reducing the on-current comprises at least one diode.

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17. (original) The Schmitt trigger of claim 16, wherein the at least one diode comprises a diode-connected PMOS transistor.

18. (original) The Schmitt trigger of claim 17, wherein the diode-connected PMOS transistor couples between a ground and a drain of the first PMOS transistor.

19. (original) The Schmitt trigger of claim 17, wherein the diode-connected PMOS transistor couples between a supply voltage terminal and a source of the first PMOS transistor.

20. (original) The Schmitt trigger of claim 19, further comprising:

a first inverter configured to invert the input voltage to provide an inverted output at an output terminal; and

a second inverter configured to invert the inverted output from the output terminal of the first inverter, wherein a drain of the first PMOS transistor couples to the output terminal of the first inverter.

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